6 Technical Data

Guaranteed values indicated in this chapter are valid for 1 year from the date of delivery. The specifications given below apply to CMC test sets equipped with a **NET-1B**, a **NET-1C** or a **NET-2** interface board.

6.1 Power Supply

The *CMIRIG-B* is powered via the "ext. Interf." connector on the CMC test set.

Table 6-1:
Power supply data

Power supply	
Supply from CMC	14 VDC
Power consumption	3 W max.
Connection	Lemo connector labeled "CMC"

A connected *CMGPS* unit is not powered by the CMC (i.e., the separate plug-in power supply is required for the *CMGPS*).

6.2 Insulation Coordination

Table 6-2:
Insulation coordination

Insulation coordination	
Circuit group A	BNC connectors on the rear side: "IRIG-B OUT", "PPX OUT", "IRIG-B/PPS IN" (common ground)
Circuit group B	16-pole Lemo connectors on the front side: "CMC" and "CMGPS" (ground connected to housing)
Insulation type group A to group B	- Working insulation - Clearance: > 1 mm - Creepage: > 1 mm - Test voltage: 1000 VDC
Insulation resistance group A to group B	1 MΩ

The *CMIRIG-B* is an SELV device (**S**afety **E**xtra **L**ow **V**oltage). It may only be connected to external devices that fulfill the SELV requirements according to the standards EN 61010-1 or IEC 61010-1. Do not connect any of the *CMIRIG-B* connectors to circuits carrying hazardous voltages.

6.3 Outputs

6.3.1 IRIG-B OUT

Table 6-3:
Output **IRIG-B OUT**

Output IRIG-B OUT	
IRIG Standard	200-04
Data format[1]	B00x (demodulated, dc level-shift) B20x (Manchester, modulated, dc level-shift)
Output characteristic	5 V (TTL), 150 mA, for 50 Ω coaxial signal distribution
Synchrophasor (PMU) testing	Configurable with or without IEEE C37.118 extensions
Connector	BNC

1. IRIG-B functionality requires a CMC test set equipped with a **NET-1B**, a **NET-1C** or a **NET-2** interface board. The support of other formats (for example, B20x - Manchester II coding) by the CMC test set depends on the *Test Universe* software version.

6.3.2 PPX OUT

PPX OUT is a configurable pulse output (X describes the pulse rate) where the active (rising) edge is in coincidence with the start of an UTC second).

Example: 1PPS (1 pulse per second: pulse rate = 1s).

Table 6-4:
Output **PPX Out**

Output PPX OUT	
Output characteristic	5 V (TTL), 150 mA, for 50 Ω coaxial signal distribution
Minimum pulse length	1 ms
Pulse rate	IRIG-B encoder: 1 s IRIG-B decoder: 0 = single, 1 ... 65535 s
Connector	BNC

6.4 Inputs

This input can be used with two different functions:

- IRIG-B input; for configuration "Trigger via IRIG-B using a CMIRIG-B" (IRIG-B decoder), see section 5.3.1 on page 21.
- PPS input; for configuration "IRIG-B Generator following PPS using a CMIRIG-B" (IRIG-B encoder); see section 5.3.3 on page 22. That is, an external PPS source is connected and IRIG-B encoder is configured.

The input is without function if a *CMGPS* synchronization unit is connected to the *CMIRIG-B*.

Table 6-5: Input **IRIG-B/PPS IN**

Input IRIG-B/PPS IN	
IRIG Standard	200-04
Data format IRIG-B IN[1]	B00x (demodulated, dc level-shift)
Input characteristic	5 V (TTL)
Min. high level	2.0 V
Max. low level	0.8 V
Input impedance	1.5 kΩ || 1 nF
Max. input voltage	6 V
Min. input voltage	-0.5 V
Min. input PPS pulse length (PPS IN)	3 µs
Synchrophasor (PMU) testing	Configurable with or without IEEE C37.118 extensions
Connector	BNC

1. IRIG-B functionality requires a CMC test set equipped with a **NET-1B**, a **NET-1C** or a **NET-2** interface board.

6.5 Timing Specifications

There are six possible configurations that select the time reference source accordingly. For details, refer to the following sections:

- 5.3.1 ”Trigger via IRIG-B using a CMIRIG-B” on page 21
- 5.3.2 ”IRIG-B Generator Master using a CMIRIG-B” on page 21
- 5.3.3 ”IRIG-B Generator following PPS using a CMIRIG-B” on page 22
- 5.3.4 ”IRIG-B Generator following GPS using a CMIRIG-B and a CMGPS” on page 22
- 5.3.5 ”IRIG-B Generator following GPS using a CMIRIG-B and a CMGPS 588” on page 23
- 5.3.6 ”IRIG-B Generator following PTPv2 using a CMIRIG-B” on page 23

The analog amplifier outputs of the CMC test set can be re-synchronized anytime with an adjustable phase relative to the time reference edge. During the time between the synchronization edges, the CMC test set uses its internal high-precision time base for signal generation.

Figure 6-1:
CMIRIG-B timing overview

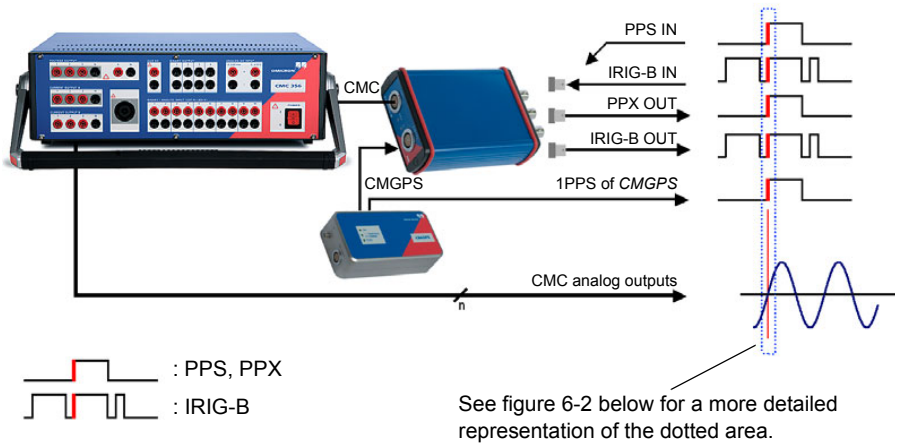


Figure 6-2:
CMIRIG-B timing in detail

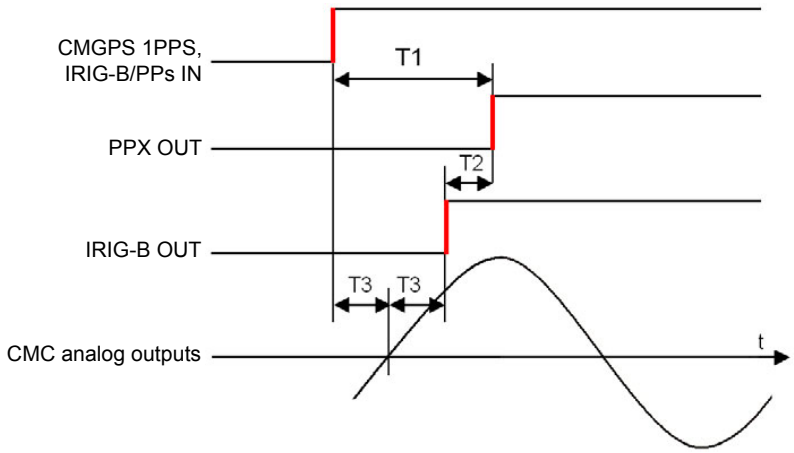


Table 6-6:
Timing specifications

Timing specifications	
T1 (delay time PPS source to PPX OUT)	< 1 µs typ., 1.5 µs max.
T2 (time skew PPX OUT to IRIG-B OUT)	< 0.1 µs typ., ± 0.5 µs max.
T3 (time error of time reference source to analog outputs)[1]	< ± 1 µs typ., ± 5 µs max.[2]

1. Applies to CMC output frequencies < 100 Hz and re-synchronized analog output signals.
2. CMC 356: < ± 5 µs typ., ± 20 µs max.

Some details regarding the timing specification:

The achievable synchronization precision of the analog CMC outputs is mainly governed by the analog signal path of the CMC hardware (analog output filters, power amplifier).

These components, together with the non-negligible but well-defined processing time in the processing unit, cause a time delay of approx. 420 µs between the numerical signal generation and the actual analog output signals. This is why the CMC output signals react with delay to the time reference (PPS, IRIG-B).

This time delay is taken into account in the signal processing in a way that (after the unavoidable initial delay) the output signals show the proper time relation (i.e., phase angle) to the time reference.

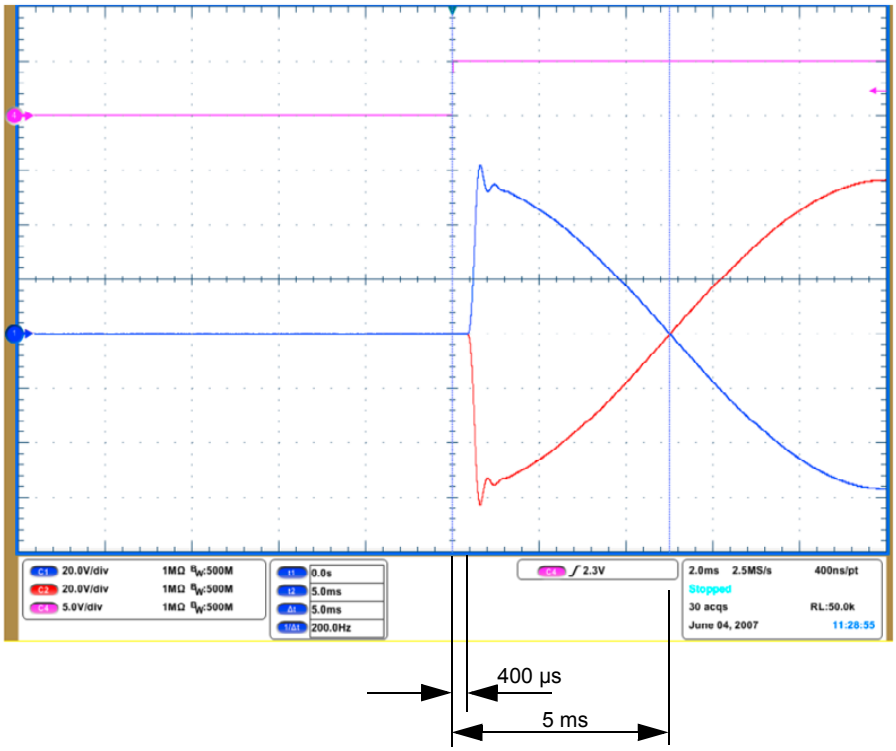
Example A: Initial synchronous start

Ch1 / blue: Amplitude step from 0 V to 40 V / 90 ° / 50 Hz

Ch2 / red: Amplitude step from 0 V to 40 V / -90 ° / 50 Hz

Ch4 / magenta: PPS (trigger)

Figure 6-3:
Example A



The time delay of approx. 400 µs caused by the analog signal path can be seen in example A (compare the amplitude step with the trigger edge). Yet the required time relation of the outputs to the reference time (PPS signal) stays untouched: The zero crossing of the analog signals occurs 5 ms after the synchronization time which is the expected behavior for a 50 Hz signal with ± 90 ° offset.

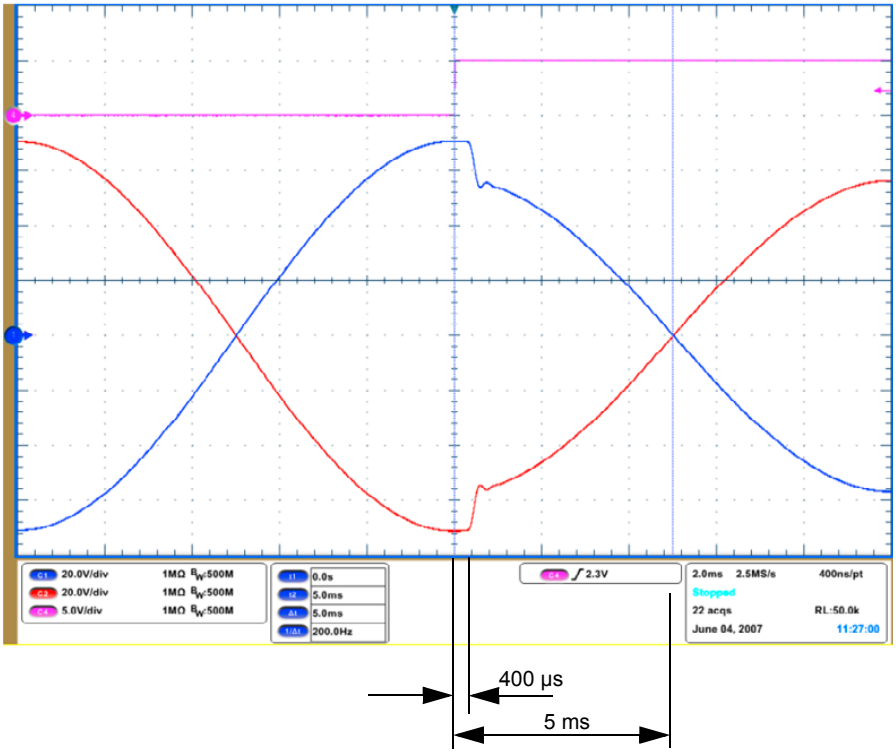
Example B: Re-synchronization with amplitude step

Ch1 / blue: Amplitude step from 50 V to 40 V / 90 ° / 50 Hz

Ch2 / red: Amplitude step from 50 V to 40 V / -90 ° / 50 Hz

Ch4 / magenta: PPS (trigger)

Figure 6-4:
Example B



The time delay of approx. 400 µs caused by the analog signal path can be observed here, too. Again, this has no influence on the phase relation between the output signals and the trigger time.

6.6 Environmental Conditions

Table 6-7: Climate conditions

Climate	
Operating temperature	0 to +50 °C (32 to +104 °F)
Storage and transportation	-25 to +70 °C (-13 to +158 °F)
Humidity	5 to 95 % relative humidity, no condensation
Max. altitude	2000 m

Table 6-8: Electromagnetic compatibility

EMC	
CE conformity, requirements	The product adheres to the guidelines of the council of the European Community for meeting the requirements of the member states regarding the electromagnetic compatibility (EMC Guidelines 89/336/EEC). EN 61326-1

Table 6-9: Fulfilled safety standards

Safety standards	
European standard	EN 61010-1:2001
International standard	IEC 61010-1:2001
ISO standard	This product is designed and manufactured under an ISO9001 registered system.

6.7 Mechanical Data

Table 6-10: Mechanical data

Size, weight and protection	
Weight	260 g (0.57 lb.)
Dimensions W x H x D	83 x 35 x 130 mm (3.3 x 1.4 x 5.1 ")
Housing	IP40 according to EN 60529

6.8 Cleaning

To clean the *CMIRIG-B* interface unit, use a cloth dampened with isopropanol alcohol or water.